Amendments to the Abstract:

Please replace the originally submitted abstract page with the following:

Hardware Support for Dual Path Branch Execution in Response to Branch Prediction Information Embedded in a Branch Instruction

ABSTRACT

A method of executing microprocessor instructions includes fetching a conditional branch instruction from a storage unit such as an instruction cache. Branch prediction information embedded in the branch instruction is detected by a fetch unit of the microprocessor. Depending upon the state of the branch prediction information, instructions from the branch-taken path and the branch-not-taken path of the branch instruction are fetched and executed. Upon executing the conditional branch instruction, the speculative results from the branch-taken path are discarded if the branch is not taken and speculative results from the branch-not-taken path are discarded if the branch is taken. The branch prediction information is compiler generated information indicative of the probability of successfully predicting the branch.